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APPLICATION FOR UNITED STATES PATENT

CCD IMAGE DETECTOR AND METHOD OF OPERATING THE SAME

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CCD IMAGE DETECTOR AND METHOD OF OPERATING THE SAME

BACKGROUND OF THE INVENTION

[0001] The present invention relates to charge coupled devices (CCDs) for use in image collection, storage and transfer, in general, and more particularly, to a CCD image detector including a buffer area array separate from an image area array and a storage area array, the buffer area array being controlled independently of the image and storage area arrays to transfer its charge contents to a read out register of the CCD, and a method of operating the same.

[0002] Charge coupled devices or CCDs are arrays of semiconductor gates formed on a substrate of an integrated circuit or chip. The gates of the CCD are operative to individually collect, store and transfer charge. When used in image applications, the charge collected and stored in each gate of the array represents a picture element or pixel of an image. A typical CCD detector used for image applications is shown in the diagram of Figure 1 and includes an image collection area 10, an image storage area 12, and a register 14 for reading out serially the pixel charges of an image one line at a time. Each of the aforementioned two areas 10 and 12 may include an array of 512x512 CCD gates, i.e. 512 lines or rows of 512 gates per row, for example. The readout register 14 includes a line of CCD gates and operates as a shift register shifting out serially the charge contents or image pixel information of a line of the collected image. Gates of the image area 10 may be operated by clock signals 16 to transfer in parallel the charge contents of the gates of one row to another vertically downward in the direction of the arrow 18. Similarly, gates of the storage area 12 are operated by clock signals 20 to transfer in parallel the charge contents of the gates of one row to another vertically downward. And, the gates of the horizontal or readout register 14 are operated by the clock signal 22 to shift out serially from right to left the charge contents of its gates over a signal line 24.

[0003] In operation, an image detector CCD gate array may be initially purged of all charge contents, then an image is collected in the form of charges in the individual gates of the image array during a predetermined integration period which may be on the order of 100 to 250 milliseconds, for example. Thereafter, the clock signals 16 and 20 operate together to transfer the current charge contents of the gates of the image area 10 to the gates of the storage area 12 line by line. This transfer process may take on the order of 512 clock pulses of approximately 3 microseconds each, for example. Once the charges representing the pixels of the collected image are stored in the storage area 12, the clock signal 20 may

continue to shift the charge contents of the gates of the storage area 12 to the readout register 14 line by line which will take considerably longer because after each new line of charge contents is transferred to the readout register 14, the clock signal 22 clocks out the charge contents (pixel information) serially which may take 512 clock pulses of on the order of 1 microsecond each, for example. So, there will be a delay of 512 microseconds between each line transfer of 512 line transfers of the storage area 12 for readout purposes.

[0004] While the foregoing described example used specific values for integration and transfer times, it is understood that these times are application dependent and may change from one application to another. Also, there are other possible methods of clocking a CCD. For example, in some image systems, there is no separate purge cycle to define the start of an integration period. Rather, a frame transfer defines the start of integration which occurs simultaneously with burst/readout cycles.

[0005] In band transfer applications of CCD detectors, only one or more bands of adjacent rows of image information or charge content need be read out from the CCD. For example, if a band of rows is 16 rows and there are six mutually exclusive bands, then the storage area 12 may be operated by the clock signal 20 to burst through the rows thereof at a rate of 1-3 microsecond per row until the first band of rows is stored in a like number of rows adjacent the read our register 14. Thereafter, the storage area 12 may be operated to clock each row of the first band into the read out register 14 with a delay of 512 microseconds per row, for example. Once the rows of the first band are clocked out of the CCD, then the storage area 12 may be operated to burst until the second band of rows is stored in the rows adjacent read out register 14 and the process repeated for the remaining five designated bands. In this case, the transfer and readout speed of the CCD is improved by a factor of at least five since the storage area 12 is clocked slowly only approximately 102 times and rapidly clocked for the remainder of lines.

[0006] When these CCD detectors are used in an environment unprotected from radiation, like in space and in some cases, in nuclear environments, for example, high energy proton and neutron radiation may penetrate the CCD array and cause phosphorous vacancy (p-v) traps in one or more gates of the CCD where unwanted charge in the form of electrons may be stored. This trapped charge may be released in an exponential manner that can be characterized by a temperature dependent release time constant τ_R which may be on the order of 270 microseconds at 0° C., for example. Since the p-v capture time is very short, the CTE, which is a measure of how much charge is transferred, is independent of how the CCD is clocked. Where the p-v trapped charge is released does depend on the manner in which the

CCD is clocked to transfer charge from gate to gate in relation to τ_R In other words, if the CCD is clocked at a rapid rate like during frame transfers from the image area to the storage area or during bursting from one band to another, for example, so that the each clock pulse is much shorter than τ_R, then the charge released from the trap will be spread uniformly over the charge contents of many gates and may easily be removed by thresholding, for example. On the other hand, if the CCD is clocked slowly, like when data is being readout through register 14, for example, so that the clock period or delay is longer than τ_R, then most of the trapped charge will be released to the next charge content being shifted through the gate. This condition will result in a shift in the image centroid in a direction opposite to the transfer direction and a degradation of the high frequency modulation transfer function (MTF) of the CCD detector. The shift in the centroid position will increase linearly with the number of slow (period $> \tau_R$) clock pulses required to read out the image.

[0007] The present invention improves the likelihood of trapped charge in one or more gates of the CCD being released over a multiplicity of charge contents (pixel information) during a charge transfer process, thus, reducing the risk of occurrence of the aforementioned problems.

SUMMARY OF THE INVENTION

[0008] In accordance with one aspect of the present invention, a charge coupled device (CCD) image detector comprises: an image area of an array of rows of gates, each gate of the image area array being operative to collect and store a charge content representative of a picture element (pixel) of an image, the rows of gates of the image area being operative concurrently by a first clock signal to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in a predetermined direction through the image area; a storage area of an array of rows of gates, each gate of the storage area array being operative to store a charge content, the rows of gates of the storage area being operative concurrently by a second clock signal to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through the storage area, the storage area array of rows disposed in the CCD detector such that a first row of the image area array of rows is adjacent a last row of the storage area array of rows to accommodate a transfer in parallel of the charge contents of the gates of the first row of the image area to the gates of the last row of the storage area, wherein the image and storage areas are operative by the first and second clock signals, respectively, to transfer the charge contents of the rows of the image area array to rows of the storage area array; a buffer area of an array of rows of

gates, each gate of the buffer area array being operative to store a charge content, the rows of gates of the buffer area being operative concurrently by a third clock signal to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through the buffer area, the buffer area array of rows disposed in the CCD detector such that a first row of the storage area array of rows is adjacent a last row of the buffer area array of rows to accommodate a transfer in parallel of the charge contents of the gates of the first row of the storage area to the gates of the last row of the buffer area, wherein the storage and buffer areas are operative by the second and third clock signals, respectively, to transfer the charge contents of the rows of the storage area array to rows of the buffer area array; and a readout register of a row of gates, each gate of the readout register being operative to store a charge content, the readout register disposed in the CCD detector such that a first row of the buffer area array of rows is adjacent the row of the readout register to accommodate a transfer in parallel of the charge contents of the gates of the first row of the buffer area to the gates of the readout register as controlled solely by the third clock signal, the row of gates of the readout register being operative concurrently by a fourth clock signal to transfer serially the charge contents of the gates thereof through the register in a predetermined direction to an output signal line.

[0009] In accordance with another aspect of the present invention, a method of operating a charge coupled device (CCD) as an image detector comprises the steps of: (a) collecting and storing charge content in gates of an image area array of rows of gates for a predetermined period of time, the charge content of the gates of the image area array representative of a picture elements (pixels) of an image frame; (b) transferring the stored charge contents of the image area array to a storage area array of rows of gates controlled by a burst of first clock pulses wherein each pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the image and storage areas in a predetermined direction; (c) transferring the charge contents of a predetermined number of adjacent rows of the storage area array to a like number of adjacent rows of a buffer area array of rows of gates controlled by a burst of second clock pulses wherein each pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the storage and buffer areas in the predetermined direction; (d) transferring in parallel the charge contents of adjacent rows through the buffer area array in the predetermined direction by a pulse of a third clock so that the charge contents of a last row of gates of the buffer area array are transferred in parallel to a row of gates in a readout register; (e) shifting out the charge contents of the gates of the readout register serially to an output of the CCD as controlled by

the pulses of a fourth clock; (f) thereafter, repeating steps (d) and (e) for each row of the predetermined number of adjacent rows of stored charge content of the buffer area array transferred from the storage area array in step (d); and (g) repeating steps (c)-(f) for each predetermined number of adjacent rows of a set of predetermined number of adjacent rows of the storage area array.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is a sketch of a typical CCD detector used for image applications.

[0011] Figure 2 is a sketch of a CCD image detector suitable for embodying the principles of one aspect of the present invention.

[0012] Figures 3A and 3B depict a flow chart of method steps for operating the CCD image detector of Figure 1 in accordance with another aspect of the present invention.

[0013] Figure 4 depicts a flow chart of method steps for alternately operating the CCD image detector of Figure 1 in accordance with another aspect of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] A charge coupled device (CCD) image detector 40 suitable for embodying the principles of the present invention is shown by the schematic of Figure 2. Referring to Figure 2, a CCD 42 includes an image area 44 of an array of rows of gates, each gate of the image area array 44 being operative to collect and store a charge content representative of a picture element (pixel) of an image. The rows of gates of the image area 44 being operative concurrently by a first clock signal CLK1 to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in a predetermined direction noted by arrow 45 through the image area 44. The term gate as used herein means a circuit configuration comprising a plurality of capacitors electrically controllable by a plurality of phases of a clock pulse. Accordingly, any circuit configuration may be used as a gate for the embodiment without deviating from the broad principles of the present invention. Also, a clock pulse of a clock signal as described herein may comprise a plurality of phases consistent with controlling the charge storage and transfer operations of the gate circuit configuration being used in the CCD.

[0015] The CCD 42 also includes a storage area 46 of an array of rows of gates, each gate of the storage area array 46 being operative to store a charge content. The rows of gates of the storage area 46 being operative concurrently by a second clock signal CLK2 to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the

predetermined direction through the storage area 46. The storage area array of rows 46 is disposed in the CCD 42 such that a first row 48 of the image area array of rows 44 is adjacent a last row 50 of the storage area array of rows 46 to accommodate a transfer in parallel of the charge contents of the gates of the first row 48 of the image area 44 to the gates of the last row 50 of the storage area 46, wherein the image and storage areas are operative by the first and second clock signals, CLK1 and CLK2, respectively, to transfer the charge contents of the rows of the image area array 44 to rows of the storage area array 46.

[0016] The CCD 42 further includes a buffer area 52 of an array of rows of gates, each gate of the buffer area array 52 being operative to store a charge content. The rows of gates of the buffer area 52 are operative concurrently by a third clock signal CLK3 to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through the buffer area 52. The buffer area array of rows 52 is disposed in the CCD detector 42 such that a first row 54 of the storage area array of rows 46 is adjacent a last row 56 of the buffer area array of rows 52 to accommodate a transfer in parallel of the charge contents of the gates of the first row 54 of the storage area 46 to the gates of the last row 56 of the buffer area 52, wherein the storage and buffer areas are operative by the second and third clock signals, CLK2 and CLK3, respectively, to transfer the charge contents of the rows of the storage area array 46 to rows of the buffer area array 52. The size of the buffer area array 52 being optimized substantially by number of rows in relation to the rows of the image area array for charge transfer efficiency performance. This optimization process will be more fully described by way of example herein below.

[0017] Further included as part of the CCD 42 is a readout or horizontal register 58 of a row of gates, each gate of the readout register 58 being operative to store a charge content. The readout register 58 is disposed in the CCD detector 42 such that a first row 60 of the buffer area array of rows 52 is adjacent the row of the readout register 58 to accommodate a transfer in parallel of the charge contents of the gates of the last row 60 of the buffer area 52 to the gates of the readout register 58 as controlled solely by the third clock signal CLK3. The row of gates of the readout register 58 being operative concurrently by a fourth clock signal CLK4 to transfer serially the charge contents of the gates thereof through the register 58 in a predetermined direction to an output signal line 62 of the detector 40.

[0018] In one embodiment, the image area 44 includes 512 rows of 512 gates per row and the charge content of each gate represents a picture element (pixel) of an image frame. The storage area 46 and the buffer area 52 of this embodiment, together include a like number of rows and gates per row to permit the charge contents of the image area 44 which represent

the pixels of a frame image to be stored in a one-to-one manner in the gates of the storage area 46 and buffer area 52. The image area 44 and likewise, the storage area 46/buffer area 52 may be divided into a plurality of bands of adjacent rows like the bands 70 and 72, for example, wherein each band of the plurality, which may be on the order of six, for example, includes a predetermined number of rows which may be on the order of 16, for example. Accordingly, for a band readout application, the buffer area 52 may be optimized substantially in size to have an equal number of rows to the predetermined number of rows of the bands. In this example, the buffer area 52 will be sized to have 16 rows. An exemplary operation of a band readout application will be described herein below in connection with the flowcharts of Figures 3A-3B.

[0019] For a full image frame readout application, the full frame image of the image area 44 and likewise, the storage area 46/buffer area 52 may be divided into a plurality of adjacent bands, each of a predetermined number of rows which may be on the order of 32, for example. Accordingly, for a full frame image readout application, the buffer area 52 may be optimized substantially in size to have a number of rows equal to the square root of the number of rows of the image area 44 rounded up to the nearest integer. For example, if the entire image frame includes 512 rows of gates, then the image area will have 512 rows of gates and accordingly, a substantially optimum buffer area 52 is sized to have 23 rows. An exemplary operation of a full image frame readout application will be described herein below in connection with the flowchart of Figure 4.

[0020] The image detector 40 further comprises a timing controller 64 for controlling the operation of the first, second, third and fourth clock signals CLK1, CLK2, CLK3 and CLK4, respectively. In one aspect of the present invention, the timing controller 64 operates the clock signals CLK1, CLK2, CLK3 and CLK4 in a predetermined sequence to purge the CCD 42 of the image detector 40 of charge contents. In another aspect of the present invention, the timing controller 64 operates the clock signals CLK1, CLK2, CLK3 and CLK4 in a another predetermined sequence to effect a readout of the charge content of a plurality of bands of rows of gates. In still another aspect of the present invention, the timing controller 64 operates the clock signals CLK1, CLK2, CLK3 and CLK4 in yet another predetermined sequence to effect a readout of the charge content of an entire image frame. More specifically, the timing controller 64 is operative to: (1) control the first, second and third clock signals CLK1, CLK2 and CLK3 concurrently to transfer the charge contents of the rows of the image area array 44 to rows of the storage area array 46 and buffer area array 52, (2) control the second and third clock signals CLK2 and CLK3 concurrently to transfer the

charge contents of the rows of the storage area array 46 to rows of the buffer area array 52, (3) control the third clock signal CLK3 to transfer in parallel the charge contents of the first row 60 of the buffer area 52 to the readout register 58, and (4) control the fourth clock signal CLK4 to transfer serially the charge contents of the gates of the readout register 58 through the register 58 in a predetermined direction noted by the arrow 66 to the output signal line 62. These and other aspects of the present invention will be explained in greater detail in the description found herein below.

[0021] The timing controller 64 may be embodied as a hardwired circuit using interconnected logic gates operated in a predetermined combinational and/or sequential manner, or as a programmable read only memory or gate array, or as a programmed microcontroller, for example. In either case, the logic flow of the timing controller 64 defines a method of operating the CCD 42 which may be described in connection with steps of a flow chart. An exemplary logic flow chart for the operation of the CCD detector 42 for a band read out application is shown in Figures 3A-3B. As described herein above, for a band readout application, the image and storage areas 44 and 46, respectively, are divided into a set or plurality of bands wherein each band includes a predetermined number of adjacent rows of charge content. Referring to Figures 3A-3B, in the initial step or block 80, the CCD 42 is purged of charge content utilizing all clock signals. While the present embodiment includes a purging step, it is understood that in some applications, no separate purge cycle prior to the step of integration or charge collection is used. Rather, a frame transfer may define the step of integration without a charge purge.

[0022] A suitable method of purging the CCD 42 includes the steps of : (a) transferring the stored charge contents of the image area array 44 to the storage area and buffer area arrays, 46 and 52, respectively, controlled by a burst of pulses from clock signals CLK1, CLK2, and CLK3 wherein each pulse transfers in parallel the stored charge contents of gates between adjacent rows through the image and storage areas in the predetermined direction 45, whereby the gates of the image area array become substantially void of charge content; (b) thereafter, transferring the charge contents of a predetermined number of adjacent rows of the storage area array 46, like 23 rows, for example, to a like number of adjacent rows of the buffer area array 52 controlled by a burst of pulses from clock signals CLK2 and CLK3 wherein each pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the storage and buffer areas in the predetermined direction 45, whereby the gates of the predetermined number of adjacent rows of the storage area 46 become substantially void of charge content; (c) transferring in parallel the charge contents of

adjacent rows through the buffer area array 52 in the predetermined direction 45 by a pulse of the clock signal CLK3 so that the charge contents of the first row of gates 60 of the buffer area array 52 are transferred in parallel to the row of gates in the readout register 58; (d) shifting out the charge contents of the gates of the readout register 58 serially to the output 62 of the CCD 42 as controlled by the pulses of the clock signal CLK4; (e) thereafter, repeating steps (c) and (d) for each row of the predetermined number of adjacent rows of stored charge content of the buffer area array 52 transferred from the storage area array in step (b); and (f) repeating steps (b)-(e) until all of the gates of the remaining areas of the CCD are void of charge content. For example, if each time step (b) is performed, 23 rows are burst transferred from the storage area 46 to the buffer area 52, then step (b) will be repeated 23 times for the storage area 46 to be void of charge contents according to this exemplary method.

[0023] After the CCD 42 has been purged of charge content in step or block 80, charge is collected and stored in the gates of the image area 44 for a predetermined period of time, like 100 milliseconds, for example, in step 82. During this time period, all clock signals remain idle. In the next step 84, the stored charge contents of the image area array 44 are transferred to the storage area array 46 and buffer area array 52 controlled by a burst of pulses from clock signals CLK1, CLK2 and CLK3 wherein each pulse of the aforementioned clock signals which may be on the order of three microseconds, for example, controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the image and storage/buffer areas in the predetermined direction 45. In step 86, the charge contents of adjacent rows of the storage area array 46 are transferred to a like number of adjacent rows of a buffer area array 52 controlled by a burst of pulses from clocks CLK2 and CLK3 wherein each pulse which also may be on the order of three microseconds, for example, controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the storage and buffer areas in the predetermined direction 45. The step 86 will continue until the first band, like band 70, for example, is transferred and stored in the buffer area 52. During the burst transfer of step 86, clock signals CLK1 and CLK4 may remain idle.

[0024] In block 88, the charge contents of adjacent rows of the buffer area 52 are transferred in parallel through the buffer area array in the predetermined direction 45 by a pulse of the clock signal CLK3 so that the charge contents of the first row of gates 60 of the buffer area array 52 are transferred in parallel to the row of gates in the readout register 58. Then, in step 90, the charge contents of the gates of the readout register 58 are shifted serially to the output 62 as controlled by the pulses of the clock signal CLK4, which may be on the order of one microsecond each, for example. Thereafter, in step 92, steps 88 and 90 are repeated until

each row of the first band of adjacent rows of stored charge content of the buffer area array 52 is transferred to and readout through the register 52. Then, in steps 94 and 96, steps 86, 88, 90, and 92 are repeated in sequence for each band of adjacent rows of the storage area 46 until all of the bands of charge content of the plurality of bands are shifted out of the CCD 42. Thereafter, in step 98 the method is repeated for a new charge content of the set of bands. The method steps may be repeated periodically for some applications.

[0025] An exemplary logic flow chart for the operation of the CCD detector 42 for a frame image read out application is shown in Figure 4. As described herein above, for a frame image readout application, the image and storage/buffer areas 44 and 46/52, respectively, are divided into a plurality of adjacent bands wherein each band includes a predetermined number of adjacent rows of charge content. If the buffer area 52 is optimized substantially for a frame image of 512 rows, for example, by taking the square root of the number of rows and rounding it up to the nearest integer. The number of rows in the buffer area will be 23 and for optimization purposes, the predetermined number or rows in each adjacent band of the frame image will be set at 23 rows. Thus, the image and storage/buffer areas may be divided into 23 bands, 22 of which containing 23 adjacent rows and 1 of which containing 6 adjacent rows, to render a total of 512 rows or the entire frame image.

[0026] In those steps of the exemplary method of Figure 4 that remain substantially the same as described for the method of Figures 3A-3B, like reference numerals are used and no further description will be provided.. Referring to Figure 4, the only steps that are different from the band readout method of Figures 3A-3B are the steps 100 and 102. Steps 80, 82, and 84 are performed in sequence bring the operational method flow to step 100 in which clock signals CLK2 and CLK3 are controlled to each produce a burst of 23 pulses to transfer the first band of 23 adjacent rows from the storage area 46 to the buffer area 52 which is sized or set to 23 rows. Thereafter, steps 88, 90 and 92 are performed in sequence to transfer the charge content of the 23 rows of the first band out from the CCD via register 58. Next, in step 102, steps 100, 88, 90 and 92 are repeated for each band of rows until all of the bands or the entire frame image are readout from the CCD. Optimizing the rows of the buffer area 52 will reduce the number of times that the steps 100, 88, 90 and 92 are repeated. After performing step 102, the method may be repeated, preferably periodically .

[0027] In an alternate embodiment, the storage area 46 of 512 rows, for example, may be divided into 16 adjacent bands of 32 adjacent rows each whereby the number of rows of the buffer area 52 may be set at 32 rows. In this example, the steps 100, 88, 90, and 92 are repeated 16 times for a complete frame image readout.

[0028] Note that according to the foregoing described exemplary methods, for a CCD image detector divided into a plurality of bands, adjacent or otherwise, the image and storage areas will incur only burst transfers controlled by pulses of approximately three microseconds each which are substantially less than the charge release time constant, thus spreading the release of any trapped charge in one or more gates over a large number of pixel charge contents. The buffer area 52 which may be optimized substantially for band and frame image readouts will incur interpulse period transfers of 512 microseconds, for example, ("slow transfer") when transferring the rows of charge content therefrom, but only for as many rows as are contained in each band, like 16 or 23 rows, for example. Note that, in the present embodiments, the storage area 46 is not clocked during the slow transfers of the buffer area 52. Only clock signal CLK3 is pulsed for these slow transfers. Storage area 46 will remain idle for the time period during which the charge contents of a band of rows is being transferred from the buffer area 52, which may be considered a slow transfer. However, the storage area 46 will incur such slow transfers only for the number of bands in a set which may be on the order of 23 or 6, for example.

[0029] Thus, in the present embodiments, the number of "slow" transfers are minimized and the number of "fast" or burst transfers are greater than in heretofore designs because the charge contents in the storage area 46 remain static during a readout of the buffer area 52. Accordingly, since the period of the "fast" transfers is much less than the trap release time constant, the release of trapped charge of a p-v trap will be spread over many charge contents or pixels with only a small amount of charge released in each following pixel in a charge transfer.

[0030] While the present invention has been described herein above in connection with a variety of embodiments, it is understood that the present embodiments are merely being presented by way of example and that the present invention should not be limited to any particular embodiment in the broadest sense. Rather, the present invention and its various aspects should be construed in breadth and broad scope in accordance with the recitation of the claims appended hereto.